Airoha Technology Corp.

AR1019
Programming Guide

Airoha Technology Corp.

Airoha Technology Corp.

HISTORY

Version	Change Summary	Date	Author
0.10	Created	14-Sep-10	Raindrop

INDEX

1 Introduction

The AR1019 FM radio single chip offers 2-wire interface for register read & write control from the host processor. The chip is controlled through register settings. In this programming guide, the pin assignment of evaluation board hardware interfaces is first introduced, followed by the detailed register description, the initialization procedure, and the detailed behavior of 2-wire interface. To help users to program code, an example(pseudo) code of AR1019 is also provided. The register map is presented at the end of this document.

Figure 1.1 shows an AR1019 EVB. The package of AR1019 is MSOP 3.0x5.0x1.1mm 10-pin package.

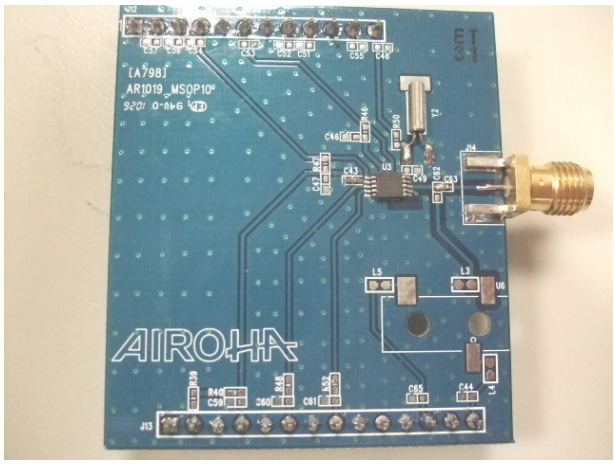


Figure 1.1: AR1019 EVB

2 Hardware Interface

There are two connectors on the AR1019 EVB: J12 and J13. The pin definitions of the two connectors are listed as follows:

PIN #	PIN Name	Description
Connector J12		
1	NC	Not connected, Keep Floating
2	NC	Not connected, Keep Floating
3	NC	Not connected, Keep Floating
4	DATAIO	Serial Interface
5	GND	Ground
6	CLOCK	Serial Interface
7	GND	Ground
8	NC	Not connected, Keep Floating
9	NC	Not connected, Keep Floating
10	NC	Not connected, Keep Floating
11	NC	Not connected, Keep Floating
12	NC	Not Connected, Keep Floating
Connector J13		
1	NC	Not connected, Keep Floating
2	NC	Not connected, Keep Floating
3	GND	Ground
4	VCC	Supply Voltage for FM Chip
5	GND	Ground
6	L_OUT	Left Channel Audio Output
7	GND	Ground
8	R_OUT	Right Channel Audio Output
9	GND	Ground
10	NC	Not Connected, Keep Floating

Please note that the Supply Voltage must be below 3.6V.

3 Register Programming Table

3.1 Register Map (AR1019)

The register map is presented at the end of this document.

3.2 Register Table (AR1019)

REG	Description
R0	
xo_en	Internal oscillator enable signal. Logic '0' for using external reference clock, logic '1' for enable the internal oscillator.
ENABLE	Analog and digital blocks enable signals.
R1	
deemp	De-emphasis. Logic '1' for 75-us de-emphasis, logic '0' for 50-us de-emphasis.
mono	Forced mono control signal. Logic '1' for mono; logic '0' depends on signal strength.
smute	Soft mute control signal. Logic '1' for enable; logic '0' for disable. Disable it when testing sensitivity.
hmute	Hard mute control signal. Logic '1' for enable; logic '0' for disable
R2	
EXT_CLK_SW	Logic'1': External reference clock mode. Logic'0': Crystal mode
TUNE	TUNE channel enable signals. '1' = Enable, '0' = Disable. Each tuning process must set this signal from '0' to '1' to get the enabling edge signal. The STC flag is cleared to '0' automatically if TUNE is set to '0'.

CHAN<9:0>	CHAN<9:1> Channel setting control signals. From 9'd0 to 9'd511. The FM channel is mapped by the equation. Frequency (MHz) = 69 + 0.1 * CHAN<9:1>. for BAND<1:0>=00, 10, 11 Frequency (MHz) = 64 + 0.1 * CHAN<9:1>. for BAND<1:0>=01 CHAN<9:0> Channel setting control signals. From 9'd0 to 9'd1023. The FM channel is mapped by the equation. Frequency (MHz) = 69 + 0.05 * CHAN<9:0>. for BAND<1:0>=00, 10, 11 Frequency (MHz) = 64 + 0.05 * CHAN<9:0>. for BAND<1:0>=01

R3

SEEKUP	Seek direction control signals. Logic '1' for seek up, logic '0' for seek down.
SEEK	SEEK channel enable signals ('1' for enable, '0' for disable). Each seeking process must set this signal from '0' to '1' to get the enabling edge signal.
SPACE	Channel spacing setting signal for SEEK operation. Logic '1' for 100k, logic '0' for 200k. When the spacing is set at 200k, no matter what the band is, it just increases or decreases it by 200k spacing.
BAND<1:0>	Band control signal. 2'b00: US/Europe band. Range from 87.5MHz to 108MHz 2'b01: 64MHz band. Range from 64MHz to 108MHz 2'b10: JAPAN band. Range from 76MHz to 90MHz 2'b11: JAPAN wide band. Range from 76MHz to 108MHz
VOLUMN<3:0>	EAR amplifier analog gain control signals while volreg_sw=0.
SEEKTH<6:0>	SEEK threshold control signals. Setting too high would result in channel missing.

R6

volreg_sw	1: Volume control is in R6 VOLUME and VOLUME2 0: Volume control is in R3 VOLUME and in R14 VOLUME2
Ear32 en_n	0: for 32 Ohm earphone: 1: Audio out to audio amplifier.
VOLUME<3:0>	EAR amplifier analog gain control signals while volreg_sw=1.
VOLUME2<3:0>	Volume control 2 while volreg_sw=1.

R7

EXT_CLK1	External reference clock setting. Please refer to Table 3.3.1. .

EXT_CLK2	External reference clock setting. Please refer to Table 3.3.1.
EXT_CLK3<2:0>	External reference clock setting. Please refer to Table 3.3.1.

R9

EXT_CLK4<8:0>	External reference clock setting. Please refer to Table 3.3.1.

R10

seek_wrap	SEEK wrap enable signal 1:wrap 0:no wrap

R11

hilo_side	AFC high side and low side injection control.
hiloctrl_b1	High side control bit 1
hiloctrl_b2	High side control bit 2

R14

VOLUME2<3:0>	Volume control 2 while volreg_sw=0.

R15

Space_50K	Channel spacing setting signal for SEEK operation. Logic '0': channel spacing depends on R3 SPACE setting (for 100k or 200k). Logic '1' for 50k channel spacing.

R16

EXT_AC_CLK	Logic '0': External DC couple reference clock. Logic '1' External AC couple reference clock.

RSSI

RSSI<6:0>	RF input signal strength
IF_CNT<8:0>	IF frequency counter

STATUS

READCHAN<9:0>	Current Channel number. Channel mapping is the same as CHAN<9:0>.
STC	Seek/Tune complete flag, '1'=Complete, '0'=Incomplete
SF	Seek fail flag, '1'=Seek Fail, '0'=Successful
ST	Stereo flag, '1'=Stereo, '0'=Mono

DEVID

VERSION<3:0>	FM radio version control (4'b0110)
MFID<11:0>	Manufacturer ID (12'h5B1)

CHIPID

CHIPNO<15:0>	FM radio IC No. (16'h1010)

Please notice that in AR1019, register address from 00H~11H are control registers and could be READ or WRITE; register address from 12H~1CH are status registers and could be READ only.

3.3 External Reference Clock setting

Different external reference clock is supported by AR1019. The register setting is as follows:

Reference Clock	EXT_CLK_SW	EXT_CLK1	EXT_CLK2	EXT_CLK3<2:0>	EXT_CLK4<8:0> (in decimal)
32.768KHz	1	0	1	3'b110	125
32KHz	1	0	1	3'b110	128
12MHz	1	1	0	3'b000	128
13MHz	1	1	0	3'b001	489
19.2MHz	1	1	0	3'b010	128
24MHz	1	1	1	3'b000	128
26MHz	1	1	1	3'b001	489
38.4MHz	1	1	1	3'b010	128
4.5MHz	1	1	0	3'b100	365
27MHz	1	1	0	3'b101	463

Table 3.3.1: External reference clock setting

For AC couple external reference clock, R16 EXT_AC_CLK is 1.
For DC couple external reference clock, R16 EXT_AC_CLK is 0.

3.4 RF Frequency Calculation

The RF frequency setting of AR1019 (100K and 200K channel spcing) is calculated as follows:

RF Frequency (in MHz) = 69 + 0.1*CHAN<9:1> for BAND<1:0>=00,10,11

RF Frequency (in MHz) = 64 + 0.1*CHAN<9:1> for BAND<1:0>=01

while CHAN<9:1> (in decimal) is D8~D0 of register R2.

The RF frequency setting of AR1019 (50K channel spcing) is calculated as follows:

RF Frequency(in MHz) = 69 + 0.05* CHAN<9:0> for BAND<1:0>=00,10,11

RF Frequency (in MHz) = 64 + 0.05* CHAN<9:0> for BAND<1:0>=01

while CHAN<9:1> is D8~D0, and CHAN<0> is D11 of register R2. CHAN<9:0> is in decimal.

The host processor can set RF frequency directly by changing CHAN values. The BAND bit (D12 and D11 of register R3) is used to indicate the valid frequency range for TUNE and SEEK functions of AR1019, 76~90MHz for Japan band and 87.5~108MHz for US/Europe band, 76~108MHz for Japan wideband and 64MHz band (64MHz~108MHz) is also supported.

3.5 Note about SEEK Function

Before a SEEK function is performed, host controller should set appropriate CHAN as the starting frequency to seek from. This value may be read from the previous seeking result in READCHAN<9:0> and be set onto CHAN<9:0>. After CHAN<9:0> is updated the SEEK function could then be enabled. STC flag should be used to check if SEEK operation is finished or not. When STC flag is set, SF flag indicates if this operation successes or not. If no station is found, SF is set to 1 which means “seek fail”. The SEEK operation under way could be stopped by register setting.
When Audio output load resistance is 32Ω, the control software should wait a delay (at least 100ms) between mute and seek/tune. Please refer to CH.6 pseudo code

3.6 Note about SEEK/TUNE with Auto Hi/Lo Side Selection

Cooperating with software driver, user can accomplish SEEK/TUNE with auto Hi-Lo Side selection. See also Chapter 6 Pseudo Code for implementation.

3.7 Default register values for variant applications

The default register values of AR1019 may be different for variant applications. Available Settings (for 32.768KHz) are listing as follows. For different external clock, some registers must be modified. Please refer to CH.3.3.

Settings	Apply To	Audio Output Load Resistance (=32Ω)*	Ref. Clock	Note
ARDSG-X1-Xtal_v002	AR1019	No	32.768 KHz Crystal	It is identical to ARF_V023_080121_MP3
ARDSG-X1-EXT_v002	AR1019	No	External 32.768KHz Clock	
ARDSG-X1-Xtal-32R_v002	AR1019	Yes	32.768 KHz Crystal	* When Audio output load resistance is 32Ω, the control software should wait a delay (at least 100ms) between mute and seek/tune. Please refer to CH.6 pseudo code
ARDSG-X1-EXT-32R_v002	AR1019	Yes	External 32.768KHz Clock	

3.8 Volume control of AR1019

The volume control of AR1019 could be set by sending registers. There are two volume control fields in registers: Volume in R3 (D7~D10), Volume2 in R14 (D12~D15) when volreg_sw=0. When volreg_sw=1, the volume control registers: Volume in R6 (D4~D7), Volume2 in R6 (D0~D3).The following table presents 19 recommended combinations to increasing the gain of L/R audio outputs.

Step	Volume2	Volume	Audio out* @ FD=22.5KHz(mVrms)
15	$1111_{(b)}$	$0000_{(b)}$	92.0
14	$1110_{(b)}$	$0000_{(b)}$	72.0
13	$1101_{(b)}$	$0000_{(b)}$	57.0
12	$1100_{(b)}$	$0000_{(b)}$	36.0
11	$1011_{(b)}$	$0000_{(b)}$	23.0
10	$1010_{(b)}$	$0000_{(b)}$	14.5
9	$1001_{(b)}$	$0000_{(b)}$	9.0
8	$1000_{(b)}$	$0000_{(b)}$	5.5
7	$0111_{(b)}$	$0000_{(b)}$	3.4
6	$0110_{(b)}$	$0000_{(b)}$	2.2
5	$0101_{(b)}$	$0000_{(b)}$	1.3
4	$0100_{(b)}$	$0000_{(b)}$	0.8
3	$0011_{(b)}$	$0000_{(b)}$	0.5
2	$0010_{(b)}$	$0000_{(b)}$	0.34
1	$0001_{(b)}$	$0000_{(b)}$	0.16
0	$0000_{(b)}$	$1111_{(b)}$	0 (mute)

*Audio output load resistance is 32Ω

4 Initialization Procedure

The serial interface is built by BUSEN, CLOCK and DATA. The 3-wire mode is selected if BUSMOD is HIGH, and the 2-wire mode is selected if BUSMODE is LOW.

Register Feeding Sequence of Power-on Initialization:

At the Register Setting Stage of AR1019 after the Reset State, the register feeding sequence must be in the following order:

AR1019 Series: (START) 01H → 02H → ⋯ → 11H → 00H (END)

And then enter the Calibration State. This order must be followed no matter 2-wire or 3-wire interface is used.

When AR1019 finishes its Calibration State, the STC flag will be set. The control software must wait for this flag before the first tune.

The timing diagrams are shown in figure 4.1 and 4.2.

Figure 4.1: Procedure for 2-wire mode initialization in AR1019

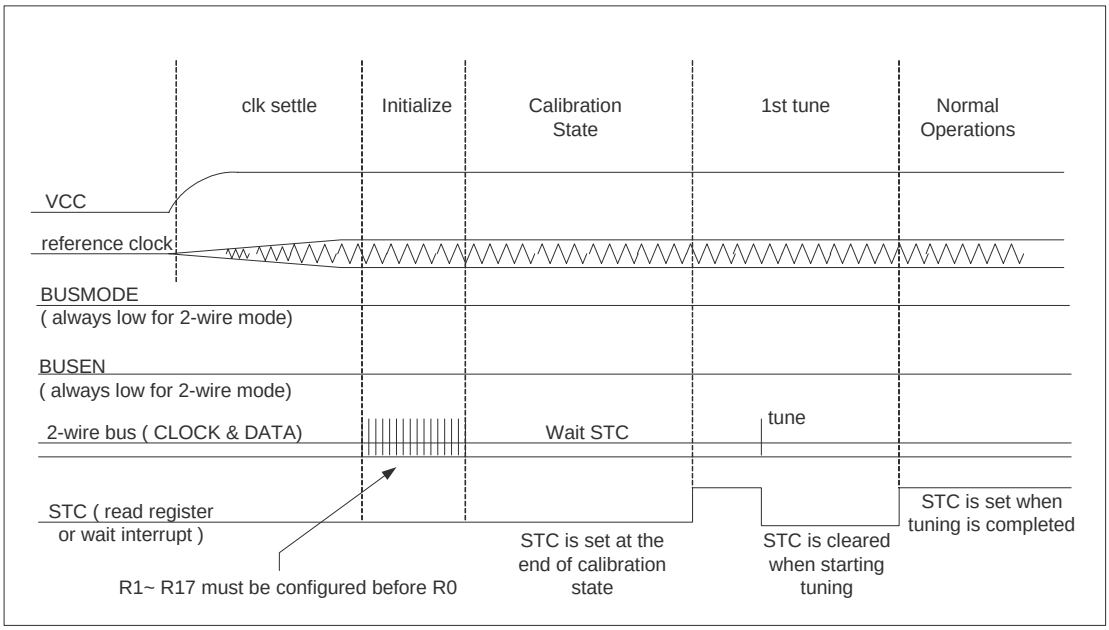
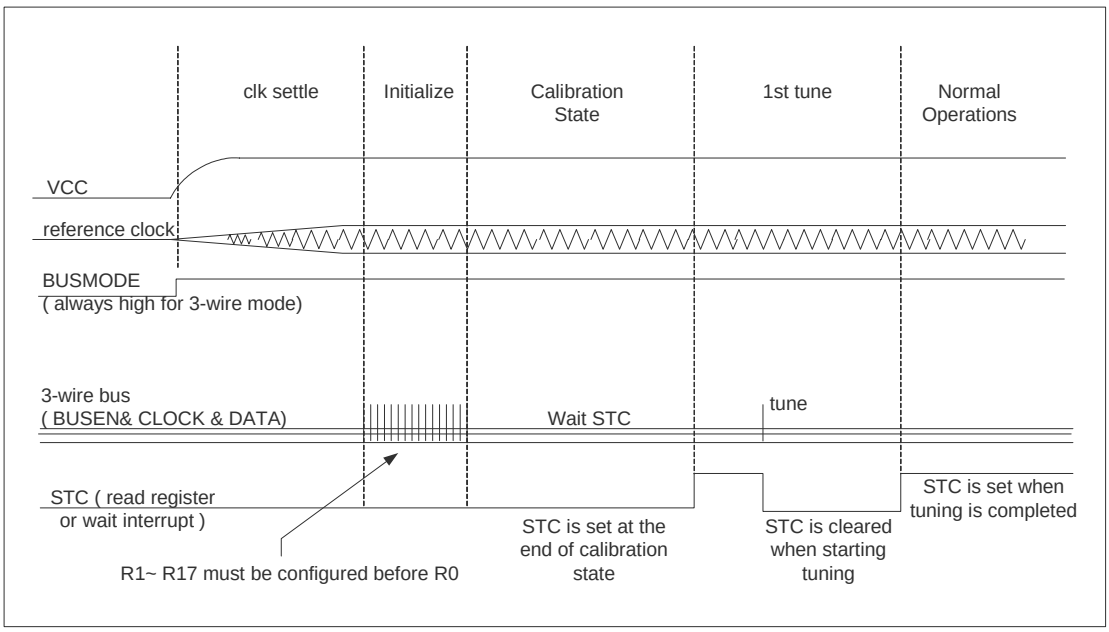


Figure 4.2: Procedure for 3-wire mode initialization in AR1019



5 Serial Interface

5.1 The 2-Wire Interface

As shown in figure 5.2.1, the data length is 8-bits long for one data transfer on 2-wire interface. Each data transfer is followed by an ACK bit from receiver side. Data is transferred with the most significant bit (MSB) first.

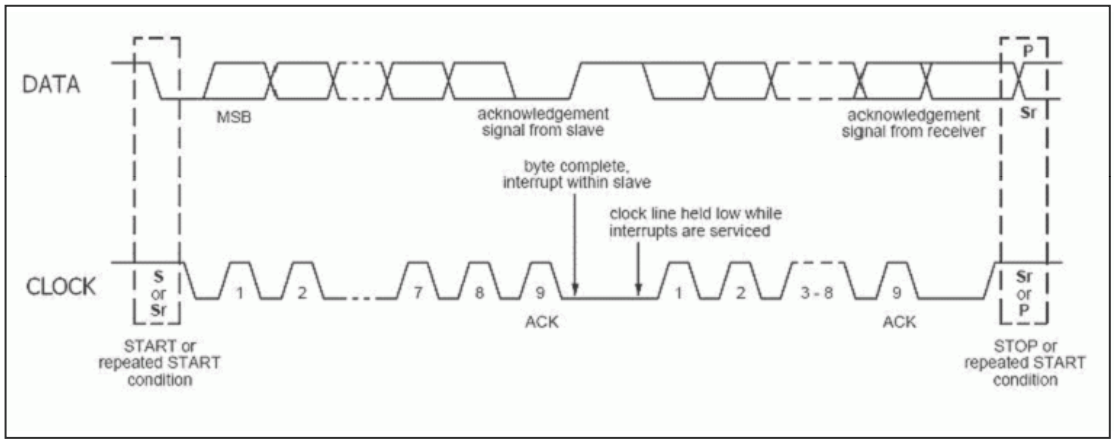


Figure 5.2.1: Data transfer on 2-wire interface

In a “READ” mode, as shown in figure 5.2.2, the receiver should send an ACK (=”0”) signal to transmitter at the end of each 8-bit data transfer, and the transmitter will send the following data. On the other hand, if the receiver sends a NACK (=”1”) signal to transmitter, the READ mode will be terminated.

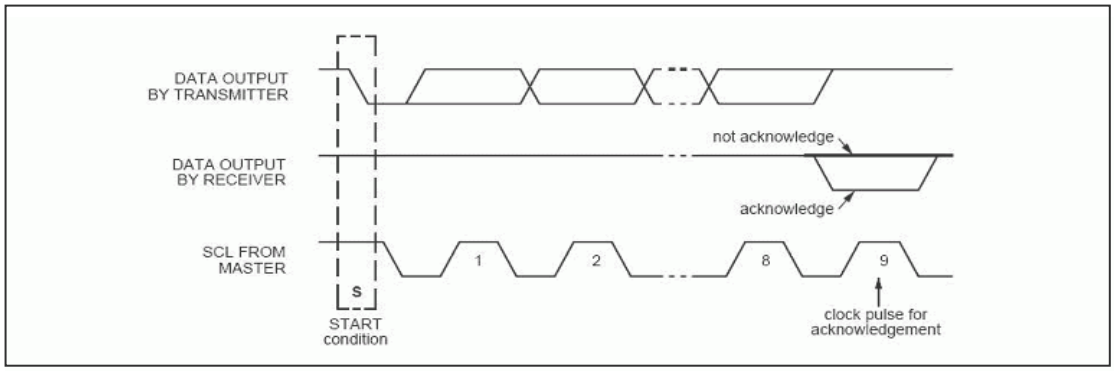


Figure 5.2.2: ACK / NACK of the 2-wire interface

In a WRITE mode, the host processor is the “master-transmitter” while AR1019 is the “slave-receiver”. In a “READ” mode, the host processor is the “master-receiver” while AR1019 is the “slave-transmitter”. The device address of AR1019 in 2-wire mode is 7b’001_0000.

Write a register into AR1019 through 2-wire interface

To write a register data into AR1019, as shown in Figure 5.2.3, the master-transmitter should at first initiate a start condition followed by the 7-bit 2-wire-mode slave address and a WRITE bit (R/$\dot{W}$=”0” which means this is a WRITE process) to indicate that AR1019 should be into WRITE mode now. The slave-receiver (AR1019) then returns an ACK to master-transmitter.

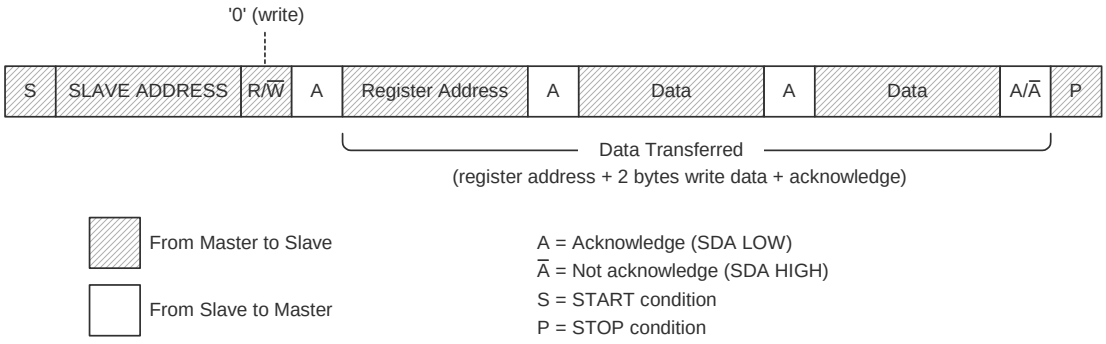


Figure 5.2.3: WRITE mode of 2-wire interface

Then master-transmitter transmits the target register address into slave-receiver, and slave-receiver returns an ACK again. The register content (16-bit length) is separated into two bytes data and sent into the slave-receiver, and slave-receiver should send back two ACK correspondingly. The whole WRITE Register process is then terminated by a STOP condition from master-transmitter.

The whole WRITE ONE REGISTER process could be designed as follows:

1. Master (Host processor) initiates a START condition.
2. Master writes the device address of the slave (AR1019), and then followed a WRITE bit. Slave sends back an ACK.
3. Master writes the register address of AR1019. Slave sends back an ACK.
4. Master writes 2-byte data to complete a register, and then sends a STOP condition to end the write procedure.

Read a register from AR1019 through 2-wire interface

To read a register data from AR1019, as shown in Figure 5.2.4, the process is separated into two partitions. At first the master-receiver initiates a start condition followed by the 7-bit 2-wire-mode slave address and a WRITE bit (R/$\dot{W}$=”0” which means this is a WRITE process), and the slave-transmitter returns an ACK. Then master-receiver transmits the target register address into slave-transmitter, and slave-transmitter returns an ACK again.

Figure 5.2.4: READ mode of 2-wire interface

After the target register address sent into AR1019, the master-receiver then re-initiates a start condition with the 7-bit 2-wire-mode slave address, but

followed with a READ bit (R/$\dot{W}$="1" which means this is a READ process), and the slave-transmitter returns an ACK. Then master-receiver sends CLOCK signal into slave-transmitter, and slave-transmitter outputs associated bit data at DATA pin. Master should send ACK at the end of each byte data. After the two-byte data transmitted completely, the READ mode could be terminated by a STOP condition or a NACK from the master-receiver.

The whole READ ONE REGISTER process could be designed as follows:

1. Master (Host processor) initiates a START condition.
2. Master writes the device address of the slave (AR1019), and then followed a WRITE bit. Slave sends back an ACK.
3. Master writes the register address of AR1019. Slave sends back an ACK.
4. Master re-initiates a start condition.
5. Master writes the device address of the slave (AR1019) again, and then followed a READ bit. Slave sends back an ACK.
6. Master sends CLOCK signal into slave, and slave outputs associated bit data at DATA pin. Master sends ACK at the end of each byte data.
7. After 2 bytes data read from slave, master sends a STOP condition to end the read procedure.

Conjunctive Read/Write Registers on AR1019

AR1019 also allows conjunctive register read/write through the 2-wire interface. Once a write or read process is started, the first register address is fed into AR1019. After 2-byte data transferred, the internal register address of AR1019 will automatically accumulated by 1. If the master does not send a STOP condition, the write/read process could be continued for further data transfer. The conjunctive R/W process would be terminated when master sends a STOP condition to slave. Slave could not terminate the R/W process itself. If the register address reaches the last one, then the address will automatically get back to the first one in the next transfer (wrap-around). The *LAST*

ADDRESS is different from READ to WRITE process, and different from version D to version E. Please notice that the register of AR1019 is 16-bit long, thus 2-byte data transfer is needed to complete one register's read/write process.

Figure 5.2.5 shows a conjunctive READ process of AR1019. Figure 5.2.6 shows a single READ/WRITE process of 2-wire interface. Figure 5.2.7 shows the timing parameters of 2-wire interface in READ/WRITE mode. The associated timing spec is shown in table 5.2.1.

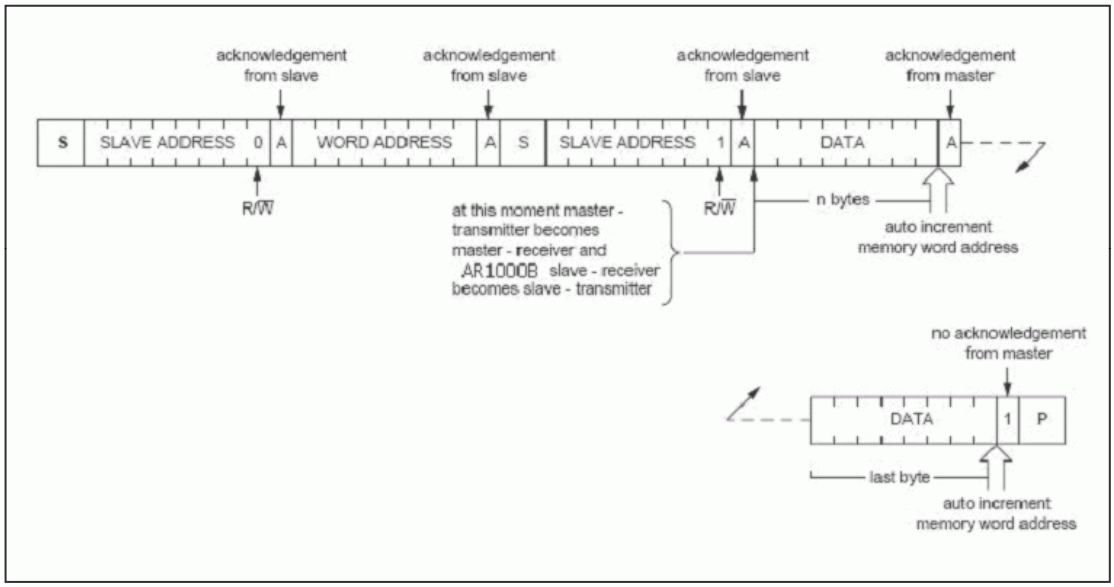


Figure 5.2.5: Conjunctive READ mode

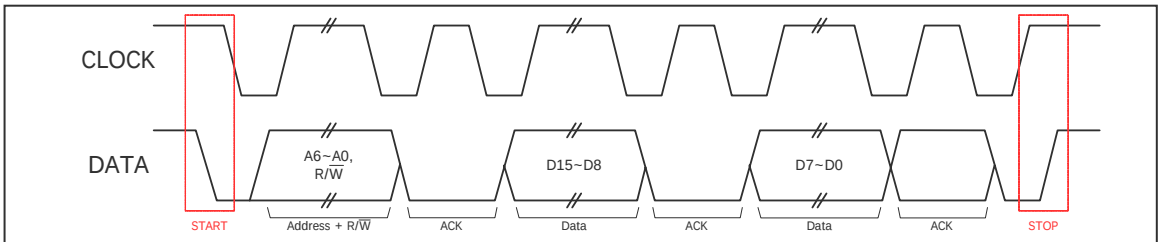


Figure 5.2.6: 2-Wire Interface Read and Write Procedure

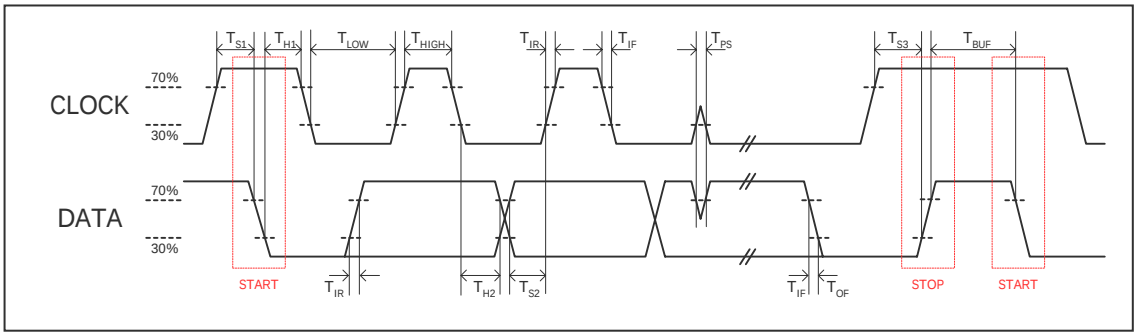


Figure 5.2.7: 2-Wire Interface Read and Write Timing Parameters

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	CLOCK Frequency	0		400	KHz
T_{S1}	CLOCK Input to DATA N-edge Setup time (START)	600			ns
T_{H1}	CLOCK Input to DATA N-edge Hold time (START)	600			ns
T_{S2}	DATA Input to CLOCK P-edge Setup time	100			ns
T_{H2}	DATA Input to CLOCK N-edge Hold time	0		900	ns
T_{S3}	CLOCK Input to DATA P-edge Setup time (STOP)	600			ns
T_{BUF}	STOP to START time	1300			ns
T_{OF}	DATA Output Fall time	20		250	ns
T_{IR}	DATA Input & CLOCK Rise time	20		300	ns
T_{IF}	DATA Input & CLOCK Fall time	20		300	ns
T_{HIGH}	CLOCK HIGH duration	600			ns
T_{LOW}	CLOCK LOW duration	1300			ns
T_{PS}	Input Filter Pulse Suppression			50	ns

Table 5.2.1: Timing parameter specs of 2-wire interface

6 Pseudo code

1. Initial

(1) Set ENABLE bit=0 (in register R0)
(2) Send default value of registers R1~R17
(3) Send default value of register R0
(4) Wait STC flag (Initialization Complete, in “Status” register)

2. Tune

(1) Set hmute Bit
(delay 100ms if audio output load resistance is 32Ω)
(2) Clear TUNE Bit
(3) Clear SEEK Bit
(4) Set BAND/SPACE/CHAN Bits
(5) Enable TUNE Bit
(6) Wait STC flag (Seek/Tune Complete, in “Status” register)
(7) Clear hmute Bit
(8) Update Functions (optional)

2. Tune with Auto Hi/Lo

(1) Set hmute Bit
(delay 100ms if audio output load resistance is 32Ω)
(2) Clear TUNE Bit
(3) Clear SEEK Bit
(4) Set BAND/SPACE/CHAN Bits
(5) Read Low-side LO Injection

1. Set R11 (clear D15, clear D0/D2)
2. Enable TUNE Bit
3. Wait STC flag (Seek/Tune Complete, in “Status” register)
4. Get RSSI (RSSI1)
5. Clear TUNE Bit

(6) Read High-side LO Injection

1. Set R11(set D15, set D0/D2)
2. Enable TUNE Bit
3. Wait STC flag (Seek/Tune Complete, in “Status” register)
4. Get RSSI (RSSI2)
5. Clear TUNE Bit

(7) Compare Hi/Lo Side Signal Strength

1. If (RSSI1 < RSSI2) Set R11(clear D15, set D0/D2), else Set R11(set D15, clear D0/D2)

(8) Enable TUNE Bit
(9) Wait STC flag (Seek/Tune Complete, in “Status” register)
(10) Clear hmute Bit
(11) Update Functions (optional)

3. Seek

(1) Set hmute Bit
(delay 100ms if audio output load resistance is 32Ω)
(2) Clear TUNE Bit
(3) Set CHAN Bits
(4) Clear SEEK Bit
(5) Set SEEKUP/SPACE/BAND/SEEKTH Bits
(6) Enable SEEK Bit
(7) Wait STC flag (Seek/Tune Complete, in “Status” register)
(8) Clear hmute Bit
(9) Update Functions (optional, but remember to update CHAN with the seek result in READCHAN before next seek)

4. Seek with Auto Hi/Lo

(1) Set hmute Bit
(delay 100ms if audio output load resistance is 32Ω)
(2) Clear TUNE Bit
(3) Set CHAN Bits
(4) Clear SEEK Bit
(5) Set SEEKUP/SPACE/BAND/SEEKTH Bits
(6) Enable SEEK Bit
(7) Wait STC flag (Seek/Tune Complete, in “Status” register)
(8) If SF is not set, tune with auto Hi/Lo (using the seek result in READCHAN as CHAN)
(9) Clear hmute Bit
(10) Update Functions (optional)

5. Update

(1) Get RSSI Bits for signal strength
(2) Get IF_CNT Bits for IF counter (ideal IF_CNT should be 256 ± 20)
(3) Get READCHAN Bits for current tuning channel

(4) Get SF Bit for Seek Failed
(5) Get ST Bit for Stereo indicator

6. Power Down (Standby mode)

(1) Clear TUNE/SEEK Bit
(2) Set ENABLE bit=0 (in register R0)

****Note: Being set ENABLE to 0, AR1019 will switch to standby mode with only very few current consumption. The complete initialization procedure can wakeup AR1019 again. After ENABLE bit is set to 1, users must wait for STC flag before tunning to the wanted frequency.**

Airoha Technology Corp.

7 Register Table

AR1019 Register Table																	
Address	Alias	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00H	R0									xo_en							ENABLE
01H	R1											stc_int_en	deemp	mono	smute	hmute	
02H	R2					CHAN<0>	EXT_CLK_SW	TUNE	CHAN<9:1>								
03H	R3	SEEKUP	SEEK	SPACE	BAND<1:0>		VOLUME<3:0>				SEEKTH<6:0>						
04H	R4																
05H	R5																
06H	R6	volreg_sw	ear32 en_n							VOLUME<3:0>				VOLUME2<3:0>			
07H	R7								EXT_CLK1	EXT_CLK2	EXT_CLK3<2:0>						
08H	R8																
09H	R9								EXT_CLK4<8:0>								
0AH	R10													seek_wrap			
0BH	R11	hilo_side													hiloctrl_b1		hiloctrl_b2
0CH	R12																
0DH	R13																
0EH	R14	VOLUME2<3:0>															
0FH	R15								SPACE_50K								
10H	R16										EXT_AC_CLK						
11H	R17																
12H	RSSI	RSSI<6:0>							IF_CNT<8:0>								
13H	STATUS	READCHAN<9:1>										STC	SF	ST			READCHAN<0>
14H	RBS																
15H	RDS1																
16H	RDS2																
17H	RDS3																
18H	RDS4																
19H	RDS5																
1AH	RDS6																
1BH	DEVID	VERSION<3:0>				MFID<11:0>											
1CH	CHIPID	CHIPNO<15:0>															
																	2010/9/14